Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A calculation unit comprising:

a parallel output N-fold shift register ~~receiving~~ configured to receive data elements to be processed where the elements are received in respective shift register folds having a predetermined fold size whereby up to N elements can be stored for parallel output from the N-fold shift register at one time;

a processor configured with a predetermined capacity for processing data vector elements and including an adder tree using a plurality of arithmetic logic unit (ALU) circuits, the processor configured to accept the output of the shift register and to provide a data output; and

the N-fold shift register configured with a selectable initial position for a data vector which exceeds the capacity of the processor and has more than N elements so as to selectively output ~~the~~ data elements based upon the capacity of the processor.

2. (Currently Amended) The calculation unit of claim 1, further comprising a multiplexer configured to receive selectively output data elements from the parallel output N-fold shift register and to selectively provide such data elements from the parallel output N-fold shift register as input to the processor ALU circuits.

3. (Currently Amended) The calculation unit of claim 2 wherein the parallel output N-fold shift register has both serial and parallel inputs further characterized by an enable circuit~~,~~ configured to selectively enable the shift register serial and parallel inputs.

4. (Currently Amended) The calculation unit of claim 1, wherein said processor is configured to process data elements that includes both real and imaginary components.

5. (Currently Amended) A calculation unit for performing a plurality of different types of calculations, the calculation unit comprising:

~~at least one~~ an input memory for storing data elements;

a parallel output N-fold shift register configured to receive data elements to be processed where the elements are received in respective shift register folds having a predetermined fold size whereby up to N elements can be stored for parallel output from the N-fold shift register at one time;

a multiplexer, for receiving the output from said shift register and providing an output to an adder tree;

the adder tree comprising a plurality of arithmetic logic units (ALUs); and

a selection circuit for selectively enabling the shift register, the multiplexer and the ~~at least one~~ input memory to apply ~~certain portions of the input~~ selected data elements to the adder tree based on the type of calculation performed.

6. (Original) The calculation unit of claim 5, further comprising, at least one selectable memory having a data width of at least a multiple of a data width of the adder tree.

7. (Currently Amended) The calculation unit of claim 1 wherein the parallel output N-fold shift register is configured to receive ~~as a selectable memory for receiving input~~ data elements from at least one input source ~~and the shift register is configured to provide a selectable output via a plurality of folds, wherein each said fold comprises at least one different position within the selectable memory~~.

8. (Currently Amended) The calculation unit of claim 7, further comprising a selectable ~~an input~~ memory configured to serve as ~~said at least one~~ an input source for the parallel output N-fold shift register and an enablement circuit to selectively control said input memory and said selectable memory depending upon the desired mathematical calculation.

9. (Previously presented) The calculation unit of claim 8, further including an accumulation circuit for receiving and selectively accumulating each output from the adder tree based on the type of calculation performed.

10. (Currently Amended) The calculation unit of claim 1 further comprising:

a memory configured to receive ~~input~~ data elements for complex resolution;

a store configured to store an operational factor for a complex function;

a multiplexer configured to selectively receive ~~input~~ data elements from the parallel output N-fold shift register via the memory or the store;

the processor ALU circuits configured as a processing array circuit, for processing data elements from selected ~~bit~~ elements locations stored by the memory and data output from the multiplexer; and

an accumulator circuit configured to receive an output from the adder tree and to provide an accumulated complex output.

11. (Cancelled)

12. (Currently Amended) The calculation unit of claim 10 a twiddle factor as the operational factor, for performing discrete Fourier transforms (DFTs), wherein the multiplexer receives its input from the store when using the twidde factor.

13.-18. (Cancelled)

19. (Currently Amended) A communication device including the calculation unit of claim 1 configured to facilitate processing of wireless communication signals wherein the parallel output N-fold shift register has more than two folds.

20. (Currently Amended) A communication device including the calculation unit of claim 5 configured to facilitate processing of wireless communication signals wherein the parallel output N-fold shift register has more than two folds.

21. (Currently Amended) A communication device including the calculation unit of claim 7 configured to facilitate processing of wireless communication signals wherein the parallel output N-fold shift register has more than two folds.

22. (Currently Amended) A communication device including the calculation unit of claim 10 configured to facilitate processing of wireless communication signals wherein the parallel output N-fold shift register has more than two folds.

23. (Currently Amended) A method of processing wireless communication signal data vectors having greater than N data elements, where N is greater than two, using a parallel output N-fold shift register configured to receive ~~that receives~~ data elements to be processed where data elements are received in respective shift register folds of a predetermined fold size whereby up to N elements can be stored for parallel output from the N-fold shift register at one time and a processor that includes an adder tree associated with a plurality of arithmetic logic unit (ALU) circuits that define a processor capacity comprising ~~characterized by~~ selectively controlling the shift register to selectively output data elements based upon the capacity of the processor and using the processor to process output data elements of the shift register ~~and~~ to thereby provide ~~a processed~~ processing of data vectors having greater than N elements.

24. (Currently Amended) The method of claim 23 further comprising using a multiplexer to receive selectively output data elements from the parallel

output N-fold shift register and to selectively provide such data elements from the parallel output N-fold shift register to the processor ALU circuits.

25. (Currently Amended) The method of claim 24 wherein the parallel output elements shift register has both serial and parallel inputs further comprising selectively enabling the shift register serial and parallel inputs based on the type of data processing computations to be performed.

26. (Currently Amended) The method of claim 25 wherein an input memory is associated with the parallel output elements shift register and the processor ALU circuits, further comprising selectively enabling input to the shift register and the processor ALU circuits from the input memory based on the type of calculation performed.

27. (Previously presented) The method claim 26 further comprising selectively enabling input from a secondary input memory to the processor based on the type of calculation performed.

28. (Currently Amended) The method of claim 27 wherein the data elements which ~~is~~ are processed ~~is~~ are data elements that includes both real and imaginary components.